Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-7. (Cancelled)

8. (New) A superscalar microprocessor for processing instructions having a sequential program order, the microprocessor comprising:

an instruction buffer configured to make a group of at least two and not more than a maximum number N of instructions concurrently available for execution, wherein the group may include up to N conditional branch instructions;

a plurality of functional units configured to execute instructions, thereby generating result data;

a register file including a plurality of entries configured to store data including result data generated by the plurality of functional units;

a decoder circuit configured to concurrently identify execution resources for more than one of the group of available instructions in the instruction buffer, the identified execution resources for each of the available instructions including a functional unit capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction;

an issue control circuit coupled to the decoder circuit and configured to concurrently issue more than one of the group of instructions from the instruction buffer to the functional units for execution, based on availability of the execution resources identified by the decoder circuit and without regard to the sequential program order;

a plurality of data routing paths coupled between the plurality of functional units and the register file and configured to concurrently transfer result data from more than one of the plurality of functional units to the register file; and

retirement control logic coupled to the register file and configured to concurrently retire a plurality of instructions according to the sequential program order.

9. (New) The microprocessor of claim 8, further comprising:

bypass control logic coupled to the plurality of data routing paths and configured to supply result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units via an alternate data path that bypasses the register file,

wherein supplying result data via the alternate data path occurs concurrently with transferring result data to the register file.

10. (New) The microprocessor of claim 8, further comprising an instruction fetch unit configured to fetch instructions from an instruction store according to the sequential program order and to transfer fetched instructions to the instruction buffer.

11. (New) The microprocessor of claim 8, wherein the instruction fetch unit includes a branch prediction circuit configured to detect a conditional branch instruction among the fetched instructions and to generate a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

12. (New) The microprocessor of claim 11, wherein the instruction fetch unit is further configured to select an instruction to be transferred to the instruction buffer subsequent, in the sequential program order, to the conditional branch instruction based at least in part on the branch bias signal.

13. (New) A method for processing instructions having a sequential program order in a superscalar microprocessor, the method comprising:

making a group of at least two and not more than a maximum number N of instructions concurrently available for execution, wherein the group may include up to N conditional branch instructions;

concurrently identifying execution resources for more than one of the group of available instructions, the identified execution resources for each of the more than one of the group of available instructions including a functional unit capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction;

concurrently issuing more than one of the group of available instructions for execution by a plurality of functional units, based on availability of the identified

execution resources for each instruction and without regard to the sequential program order;

executing the issued instructions in the plurality of functional units, thereby generating result data;

transferring the result data from the functional units to a register file, the register file including a plurality of entries; and

retiring instructions according to the sequential program order.

14. (New) The method of claim 13, further comprising, concurrently with the act of transferring, bypassing the result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units.

15. (New) The method of claim 13, wherein the act of making the group of instructions available includes fetching instructions from an instruction store according to the sequential program order.

16. (New) The method of claim 15, further comprising:

detecting a conditional branch instruction among the fetched instructions; and

generating a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

17. (New) The method of claim 16, wherein the act of making the group of instructions available includes selecting and making available an instruction that is subsequent, in the sequential program order, to the conditional branch instruction, wherein the selection is based at least in part on the branch bias signal.

18. (New) A computer system, comprising:

a memory;

a superscalar microprocessor for processing instructions having a sequential program order; and

a bus coupled between the memory and the microprocessor,

wherein the microprocessor includes:

an instruction buffer configured to make a group of at least two and not more than a maximum number N of instructions concurrently available for execution, wherein the group may include up to N conditional branch instructions;

a plurality of functional units configured to execute instructions, thereby generating result data;

a register file including a plurality of entries configured to store data including result data generated by the plurality of functional units;

a decoder circuit configured to concurrently identify execution resources for more than one of the group of available instructions in the instruction buffer, the identified execution resources for each of the available instructions including a functional unit

capable of executing the instruction and a register file entry corresponding to a source of an operand for the instruction;

an issue control circuit coupled to the decoder circuit and configured to concurrently issue more than one of the group of instructions from the instruction buffer to the functional units for execution, based on availability of the execution resources identified by the decoder circuit and without regard to the sequential program order;

a plurality of data routing paths coupled between the plurality of functional units and the register file and configured to concurrently transfer result data from more than one of the plurality of functional units to the register file; and

retirement control logic coupled to the register file and configured to concurrently retire a plurality of instructions according to the sequential program order.

19. (New) The system of claim 18, wherein the microprocessor further includes:

bypass control logic coupled to the plurality of data routing paths and configured to supply result data from a first one of the plurality of functional units as operand data for any one or more of the plurality of functional units via an alternate data path that bypasses the register file,

wherein supplying result data via the alternate data path occurs concurrently with transferring result data to the register file.

20. (New) The system of claim 18, wherein the microprocessor further includes an instruction fetch unit configured to fetch instructions from an instruction store according

to the sequential program order and to transfer fetched instructions to the instruction buffer.

21. (New) The system of claim 20, wherein the instruction fetch unit includes a branch prediction circuit configured to detect a conditional branch instruction among the fetched instructions and to generate a branch bias signal indicating whether the conditional branch is predicted to be taken or not taken.

22. (New) The system of claim 21, wherein the instruction fetch unit is further configured to select an instruction to be transferred to the instruction buffer subsequent, in the sequential program order, to the conditional branch instruction based at least in part on the branch bias signal.